KIOXIA

Technical Brief

Tech Brief Series: Analyzing Managed Flash Device[1] Lifetime Reliability

Part 1: The Fundamentals of TBW, WAF and NAND Flash Memory Endurance

This technical brief is for managed flash device customers that want to conduct a proper reliability analysis on their own covering Terabytes[2] Written (TBW), Write Amplification Factor (WAF) and NAND flash memory endurance. Once a customer gains this knowledge, they can reach out to KIOXIA for additional analysis and support to help enhance the customer's e-MMC[3] or UFS[4] device design capabilities.

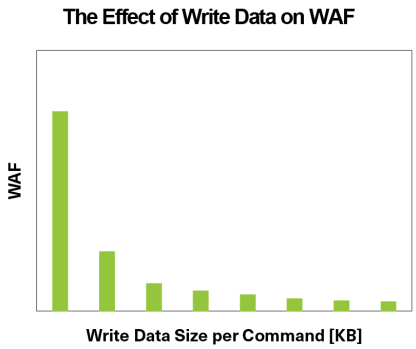
The first installment in this new series, 'Analyzing Managed Flash Device Lifetime Reliability,' covers TBW, WAF and NAND flash memory endurance. Subsequent installments are planned to cover the primary NAND flash memory reliability factors of concern when designing managed flash devices, ways to counter these reliability concerns, and the steps required for a proper lifetime reliability analysis.

TBW and WAF

TBW is a metric used in SSDs and recently in e-MMC and UFS devices. Managed flash device manufacturers use TBW to specify how much data can be written to a device before it reaches its useful end of life. An option for determining the total managed flash device endurance is to multiply its density by its maximum Program/Erase (P/E) cycle count, commonly referred to as TBW. The estimated TBW result can help to predict the amount of data (in terabytes) that can be written to a managed flash device before it may fail. It is based upon the predictability of flash memory endurance which decreases linearly as the device is written to over its lifetime as depicted by the following TBW formula:

$$\text{TBW} = \frac{\text{Terabytes Written}}{\frac{\textit{Flash Memory Maximum P/E Cycles} \times \textit{Flash Memory Density}}{\textit{WAF}}}$$

When calculating TBW, WAF is a consideration. The higher the WAF is, the lower the TBW will be. WAF is an estimation formula used to help define the ratio of physical writes[5] made to flash memory, divided by the logical writes delivered from the host. It is dependent on the workload or, essentially, the size of data written from the host. In general, small block oriented write operations to random logical block address (LBA) locations will have a higher WAF than larger block oriented writes to a sequential block address per the image below:

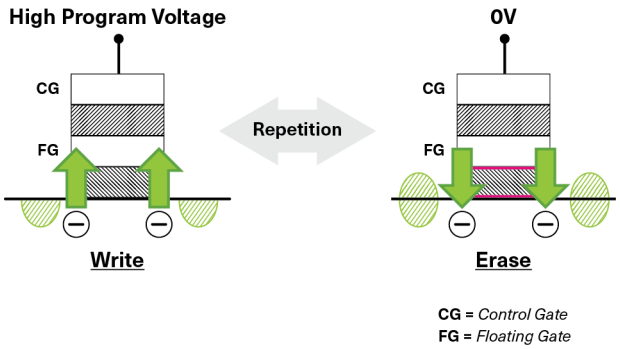


If customers are interested in the TBW of an e-MMC or UFS device, they would need to calculate the WAF for that specific application. If the TBW is published in a product specification, the supplier would typically use either a defined JEDEC® workload or a vendor-specific workload. Using the actual customer workload is the most accurate option, and is recommended for determining the TBW of an e-MMC or UFS device.

The controller for managed flash devices can be programmed to use algorithms that verify if the device access is TBW and WAF optimized. These algorithms are designed so that the flash memory cells are fully utilized, logging and system data overhead are minimized, and background maintenance work (such as garbage collection) can function at the proper timing. Understanding the algorithm employed by the managed flash device is very helpful for aligning the writing or erasing conditions. This knowledge can lead to better TBW and WAF results, which in turn can provide longer managed flash device lifecycles. For further information about TBW and WAF, download the KIOXIA tech brief entitled, "Understanding TBW versus P/E Cycles in Managed Flash Memory,' available here.

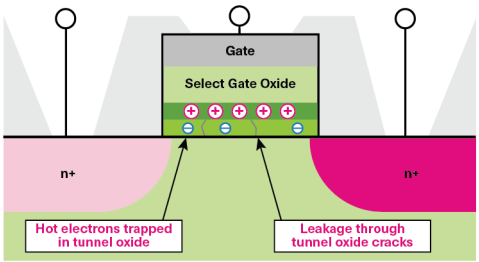
NAND Flash Memory Endurance

NAND flash memory endurance is linked to P/E cycles. It is a measurement of how many times that a NAND flash memory cell can be written to and erased before it becomes unreliable. A cell must be erased first before data can be written to it. The cycle of programming (writing) and erasing slowly degrades the cell's transistor material properties over time until the cell can no longer hold a reliable charge as presented below:

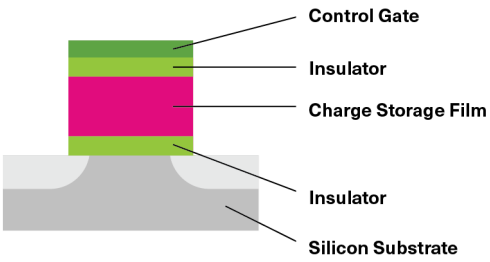


NAND flash memory has a finite number of P/E cycles before it begins to experience reliability issues. In floating gate NAND technology, electrons can be trapped in the oxide layer between the gate and substrate over time as more P/E cycles are exerted. Also, the oxide layer can crack and electrons stored in the floating gate can leak out as presented below:

NAND Flash Memory Cell Wear Out



These wear out effects can result in reliability problems that include data corruption or data loss when trying to read from flash memory, as well as program errors since data written to flash memory could be in an incorrect charge state. With the more recent advent of 3D NAND technology, manufacturers have moved from floating gate to charge trap technology as presented by the image below. Charge trap uses a non-conductive layer to trap electrons and has become a replacement for floating gate. However, the insulator will also degrade over time resulting in a finite number of P/E cycles.



The manufacturers of NAND flash memory often characterize endurance for each generation node by the number of P/E cycles supported. To maximize managed flash memory endurance, techniques such as Error Correction Coding (ECC) and wear leveling are applied.

ECC mitigates reliability issues as P/E cycles increase and it attempts to correct errors that occur if the flash cells become unreliable. In doing so, premature failures minimize enabling each cell to achieve its specified P/E cycle life expectancy.

Wear leveling is a capability where the controller manages the erase count of each block and writes data to blocks with lower values. This endurance technique distributes write operations evenly amongst specific blocks, keeping these blocks active and preventing them from deteriorating, thereby extending flash cell lifespans.

Summary

This first installment in the 'Analyzing Managed Flash Device Lifetime Reliability' series covers a general understanding of TBW, WAF and NAND flash memory endurance for customers that want to conduct a proper reliability analysis on their own. Once the analysis is completed, KIOXIA can provide free technical consultation of the customer's results to help enhance their managed flash device design capabilities.

Then next installment in this series, "Part 2: Understanding Data Retention" details key reliability concerns associated with TBW, WAF and NAND flash memory endurance.

General information for KIOXIA memory products is available here.

FOOTNOTES:

[1] A managed flash device combines raw NAND flash memory and an intelligent controller in one integrated package, enabling internal memory management.

[2] Definition of capacity - KIOXIA Corporation defines a megabyte (MB) as 1,000,000 bytes, a gigabyte (GB) as 1,000,000,000 bytes, a terabyte (TB) as 1,000,000,000,000 bytes and a petabyte (PB) as 1,000,000,000,000,000 bytes. A computer operating system, however, reports storage capacity using powers of 2 for the definition of 1Gbit = 2^{30} bits = 1,073,741,824 bits, 1GB = 2^{30} bytes = 1,073,741,824 bytes, 1TB = 2^{40} bytes = 1,099,511,627,776 bytes and 1PB = 2^{40} bytes = 1,125,899,906,842,624 bytes and therefore shows less storage capacity. Available storage capacity (including examples of various media files) will vary based on file size, formatting, settings, software and operating system, and/or pre-installed software applications, or media content. Actual formatted capacity may vary.

[3] Embedded MultiMediaCard (e-MMC) is a specification developed by JEDEC for mobile applications. The current release is v5.1, published in February 2015.

[4] Universal Flash Storage (UFS) devices are based on the UFS specification, of which, the v4.0 specification is the current release issued by JEDEC and published in August 2022.

[5] Physical writes can be obtained through the managed flash device health information.