KIOXIA

Technical Brief

Tech Brief Series: Analyzing Managed Flash Device[1] Lifetime Reliability

Part 2: Understanding NAND Flash Memory Data Retention

In today's connected world, data is stored on millions of devices around the globe each day. Sometimes that data is overwritten with new data, and is stored for a short or long time. For the latter case, the stored data should remain intact forever in an ideal world. The family photos stored on an SSD in a PC or laptop should be viewable from that same SSD for decades. Unfortunately, the laws of physics still challenge today's NAND flash memory storage and there is a finite amount of time that stored data will remain uncorrupted, a characteristic referred to as data retention.

This tech brief presents pertinent reliability factors necessary for an accurate NAND flash memory device lifetime reliability analysis and unfolds the mechanisms that influence data retention time in NAND flash memory. This is the second part in the KIOXIA 'Analyzing Managed Flash Device Lifetime Reliability Series.' In Part 1, Terabytes[2] Written (TBW), Write Amplification Factor (WAF) and Program/Erase (P/E) endurance were analyzed in detail.

Data Retention Overview

From a NAND flash memory perspective, data retention is the amount of time that data can be reliably stored in a specific address location without corruption. It is a pertinent reliability factor that can change the bit value and cause corruption to stored data. Data retention time for a NAND flash memory cell is highly influenced by the P/E cycle count and the ambient temperature surrounding the part. Figure 1 displays a Triple-Level Cell[3] (TLC) NAND flash memory cell's voltage distributions representing various bit patterns of data that can be stored in the cell.

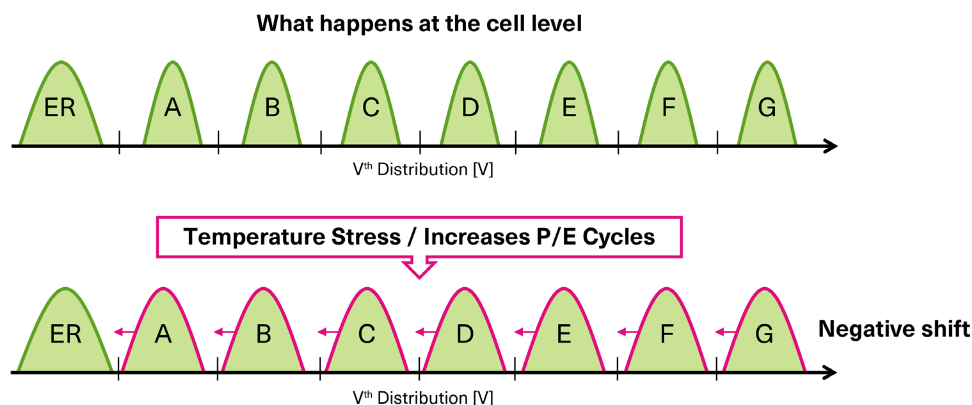

Figure 1 depicts the voltage distribution of a TLC NAND flash memory cell

The threshold voltage level (V^{th}) stored in the cell's transistor determines the bit information stored in the cell itself. The top diagram in Figure 1 shows cell threshold voltage distribution (V^{th} distribution) at the beginning of cell life, and evenly spaced with peaks at appropriate voltages. The bottom diagram in Figure 1 shows the effects on cell threshold voltage once temperature stress and an increase in P/E cycles become evident. As the threshold voltage distribution becomes wider and negatively shifts over time, the probability for bit corruption increases.

NAND Flash Memory Data Retention Analysis

When designing applications with NAND flash memory, data retention is a very important consideration that requires analysis. In general, when NAND flash memory accumulates more P/E cycles and experiences higher ambient temperature, data retention time will be shorter. Therefore, it is important to estimate data retention time at the end of system lifetime by comparing the P/E cycle count with the data retention characteristics at the ambient temperature of the use case in question.

Figure 2 is an output plot showing a general relationship between data retention time, P/E cycles and ambient temperature at the NAND flash memory cell level. It depicts how an increase in the P/E cycle count, and/or an increase in the ambient temperature, will shorten the retention time of the data in that cell. The dashed vertical ‘Spec’ line refers to the NAND flash memory P/E count threshold specification or essentially the point when uncorrected errors can occur if any additional P/E cycles are accumulated. The three colored lines in Figure 2 represent three ambient temperatures (low, mid and high).

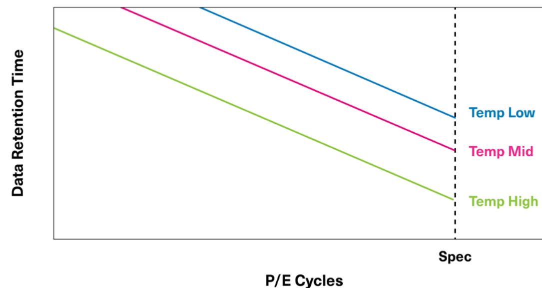

Figure 2 is a general example that shows the relationship between data retention time, P/E cycles and ambient temperature

As such, data retention values come from the supplier and are generally not measurable by the user. KIOXIA can help customers better understand the effects of data retention and endurance in their application. If the estimated data retention time does not meet system requirements, there are mitigation techniques to extend data retention time through the life of the system.

Summary

This second installment in the ‘Analyzing Managed Flash Device Lifetime Reliability’ series covers NAND flash memory data retention and the amount of time that data can be reliably stored without corruption. As a charge may gain or be lost in a transistor over time, the voltage distributions become wider and negatively shift - causing bit values to change and resulting in corrupted stored data.

Data retention time for a NAND flash memory cell is highly influenced by the P/E cycle count and the ambient temperature surrounding the part. Once the maximum P/E cycle count and ambient temperature profile are determined, the supplier can perform a calculation of the user’s worst case of data retention value.

Part 3 in this series will focus on using various refresh operations to protect data retention in NAND flash memory.

General information for KIOXIA memory products is available here.

FOOTNOTES:

[1] A managed flash device combines raw NAND flash memory and an intelligent controller in one integrated package, enabling internal memory management.

[2] Definition of capacity - KIOXIA Corporation defines a megabyte (MB) as 1,000,000 bytes, a gigabyte (GB) as 1,000,000,000 bytes, a terabyte (TB) as 1,000,000,000,000 bytes and a petabyte (PB) as 1,000,000,000,000,000 bytes. A computer operating system, however, reports storage capacity using powers of 2 for the definition of 1Gbit = 2^{30} bits = 1,073,741,824 bits, 1GB = 2^{30} bytes = 1,073,741,824 bytes, 1TB = 2^{40} bytes = 1,099,511,627,776 bytes and 1PB = 2^{40} bytes = 1,125,899,906,842,624 bytes and therefore shows less storage capacity. Available storage capacity (including examples of various media files) will vary based on file size, formatting, settings, software and operating system, and/or pre-installed software applications, or media content. Actual formatted capacity may vary.

[3] Triple-Level Cell (TLC) NAND flash memory stores three bits per cell. Additional NAND flash memory classes include Single-Level Cell (SLC) that stores one bit per cell, Multi-Level Cell (MLC) that stores two bits per cell and Quad-Level Cell that stores four bits per cell

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